Please amend the application as provided below.

THE TITLE

Please replace the title with --**Method of Making a Memory Cell with Polished Insulator Layer**--.

IN THE CLAIMS

The following is a clean version of the entire set of pending claims. In accordance with 37 CFR §1.121(c)(1)(ii), Attachment A provides marked up versions of the claims containing the newly introduced changes.

1. (Twice Amended) A method of making a flash memory cell including a substrate and a floating gate, the method comprising:

depositing an insulator layer of high temperature oxide on the substrate and the floating gate, the insulator layer being deposited to a thickness greater than a thickness of the floating gate, and operable to prevent charge leaking from the floating gate;

polishing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

3. The method of claim 1, wherein the thickness of the floating gate is between approximately 500Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

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4. The method of claim 1, wherein polishing the insulator layer includes chemical mechanical polishing.

5. The method of claim 1, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

6. The method of claim 5, wherein depositing the dielectric layer includes depositing an ONO layer.

7. (Twice Amended) A method of making a flash memory cell having a substrate and a tunnel oxide formed on the substrate, the method comprising:

depositing a floating gate layer on the tunnel oxide to a first thickness;

etching the floating gate layer, to provide a floating gate;

depositing an insulator layer of high temperature oxide on the substrate and the floating gate such that the insulator layer has a thickness that is greater than the first thickness;

polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer; and

depositing a dielectric layer on the planar surface directly over the exposed top surface of the floating gate and the insulator layer.

9. The method of claim 7, wherein the first thickness is between approximately 500 Å and 2000 Å, and the thickness of the insulator layer, when deposited, is between approximately 1000 Å and 5000 Å.

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10. The method of claim 7, wherein polishing the insulator layer includes chemical mechanical polishing.

11. The method of claim 7, further comprising:

depositing a control gate layer on the dielectric layer; and

etching the control gate layer and the dielectric layer to form a stacked gate structure of the flash memory cell.

12. The method of claim 11, wherein depositing the dielectric layer includes depositing an ONO layer.

13. (Canceled)

14. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped polysilicon.

15. The method of claim 7, wherein depositing the floating gate layer includes depositing a doped amorphous silicon.

REMARKS

The title has been amended in compliance with the Examiner's suggestion. Claims 1-12, 14 and 15 are pending. Claims 2 and 8 are cancelled by virtue of this amendment. Claims 1 and 7 are amended. Thus, claims 1, 3-7, 9-12, 14 and 15 are pending for the Examiner's consideration.

Claims 1 and 7 are rejected by the Examiner under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Claims 1-12, 14 and 15 are

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